In the claims:

1. (Original) A DRAM circuit comprising a plurality of aligned sense amplifiers,

bit line pairs connected to the plurality of sense amplifiers, respectively, and

memory cells connected respectively to the bit lines constituting the bit line pairs, wherein

the bit line pairs and the memory cells are alternately arranged on a right side (upper side) and a left side (lower side) of the sense amplifiers per N (N: natural number) aligned sense amplifiers.

2. (Original) The DRAM circuit according to claim 1, wherein there cross two bit lines constituting the bit line pair arranged on one side of a right side (upper side) and a left side (lower side) of the sense amplifier, and a space between the bit lines widens or narrows from the cross.

3. (Original) The DRAM circuit according to claim 2, wherein, further, two bit lines constituting the bit line pair, which is arranged on the other side of the one right side (upper side) or left side (lower side) of the sense amplifier, do not cross, and a space therebetween widens or narrows on the way.

4. (Original) The DRAM circuit according to claim 1, wherein the bit line pairs arranged on one of the right side (upper side) and left side (lower side) of the sense amplifier are both connected to corresponding data lines via bit switches.

PAGE 4/18 * RCVD AT 2/1/2005 2:47:45 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/6 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):04-48

5. (Original) The DRAM circuit according to claim 1, wherein the plurality of aligned sense amplifiers is divided every M sense amplifiers (M: natural number), and a set driver is disposed in a separated area.

6. (Original) The DRAM circuit according to claim 3, wherein the bit line pairs comprise a bit line configuration in a multiple twisted bit line (MTBL) method.

7. (Original) A DRAM circuit comprising:

a plurality of sense amplifiers arranged in Q lines each containing the P sense amplifiers;

bit line pairs connected to the plurality of sense amplifiers, respectively; and

memory cells connected respectively to the bit lines constituting the bit line pairs,

wherein the bit line pairs and the memory cells are arranged every N (N: natural number) aligned sense amplifiers in the Q lines, alternately on a right side (upper side) and a left side (lower side) of the sense amplifiers, and P and Q are both integers of more than 3, and N is an arbitrary integer of more than 1 and less than (P/3).

8. (Currently amended) A DRAM circuit comprising a plurality of sense amplifiers SA (J, K) arranged in Q lines each containing the P sense amplifiers,

bit line pairs connected to the plurality of sense amplifiers SA (J, K), respectively, and

memory cells connected respectively to the bit lines constituting the bit line pairs, wherein

PAGE 5/18 * RCVD AT 2/1/2005 2:47:45 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/6 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):04-48

the sense amplifier SA (J, K) is connected to each of the bit line pairs arranged between the sense amplifier SA (J, K) and a sense amplifier SA (J, K-1) in one next line ~~or a sense amplifier SA (J, K+1) in the other next line~~;

a sense amplifier SA (J+1, K) is connected to the bit line pairs arranged between the sense amplifier SA (J+1, K) and a sense amplifier SA (J+1, K+1) in another ~~one next line or a sense amplifier SA (J+1, K-1) in the other~~ next line;

a sense amplifier SA (J+2 ~~3~~, K) is connected to each of the bit line pairs arranged between the sense amplifier SA (J+2 ~~3~~, K) and a sense amplifier SA (J+2, K-1) in one next line ~~or a sense amplifier SA (J+2, K+1) in the other next line~~; and

P and Q are both integers of more than 3, J is an arbitrary integer of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q.

9. (Currently amended) The DRAM circuit according to claim 8, wherein two bit lines constituting the bit line pair, which is arranged in one space between the sense amplifier SA (J, K) and the sense amplifier ~~SA (J, K+1) or~~ SA (J, K-1) in the next line, cross, and from the cross, a space between the two bit lines widens or narrows.

10. (Currently amended) A DRAM circuit comprising a plurality of sense amplifiers SA (J, K) arranged in Q lines each containing the P sense amplifiers,

bit line pairs connected to the plurality of sense amplifiers SA (J, K), respectively, and

memory cells connected respectively to the bit lines constituting the bit line pairs, wherein

PAGE 6/18 * RCVD AT 2/1/2005 2:47:45 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/6 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):04-48

the sense amplifier SA (J, K) is connected to each of the bit line pairs arranged between the sense amplifier SA (J, K) and a sense amplifier SA (J, K-1) in one next line or a sense amplifier SA (J, K+1) in the other next line;

a sense amplifier SA (J+1, K) is connected to the bit line pairs arranged between the sense amplifier SA (J+1, K) and a sense amplifier SA (J+1, K+1) in one next line or a sense amplifier SA (J+1, K-1) in the other next line;

a sense amplifier SA (J+3, K) is connected to each of the bit line pairs arranged between the sense amplifier SA (J+3, K) and a sense amplifier SA (J+2, K-1) in one next line or a sense amplifier SA (J+2, K+1) in the other next line; and

P and Q are both integers of more than 3, J is an arbitrary integer of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q, wherein two bit lines constituting the bit line pair, which is arranged in one space between the sense amplifier SA (J, K) and the sense amplifier SA (J, K+1) or SA (J, K-1) in the next line, cross, and from the cross, a space between the two bit lines widens or narrows and ~~The DRAM circuit according to claim 9,~~ wherein, further, two bit lines constituting the bit line pair, which is arranged in a space opposite to the one space between the sense amplifier SA (J, K) and the sense amplifier SA (J, K+1) or SA (J, K-1) in the next line, do not cross, and a space therebetween widens or narrows on the way.

11. (Currently amended) The DRAM circuit according to claim 8, wherein the bit line pairs arranged in one space between the sense amplifier SA (J, K) and the sense amplifier ~~SA (J, K+1) or~~ SA (J, K-1) in the next line are both connected to corresponding data lines via bit switches.

12. (Original) The DRAM circuit according to claim 8, wherein the plurality of sense amplifiers, whose number arranged in one line is P, is divided every M sense amplifiers (M: natural number), and a set driver is disposed in a separated area.

PAGE 7/18 * RCVD AT 2/1/2005 2:47:45 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/6 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):04-48

13. (Original) The DRAM circuit according to claim 10, wherein the bit line pairs comprise a bit line configuration in a multiple twisted bit line (MTBL) method.

14. (Currently amended) A DRAM circuit comprising:

a plurality of sense amplifiers SA (J, K) arranged in Q lines each containing the P sense amplifiers;

bit line pairs connected to the plurality of sense amplifiers SA (J, K), respectively; and

memory cells connected respectively to the bit lines constituting the bit line pairs,

wherein the sense amplifier SA (J, K) and a sense amplifier SA (J+1, K) are each connected to each of the bit line pairs arranged between a sense amplifier SA (J, K-1) in one next line and a sense amplifier SA (J+1, K-1) ~~or between a sense amplifier SA (J, K+1) in the other next line and a sense amplifier SA (J+1, K+1)~~;

a sense amplifier SA (J+2, K) and a sense amplifier SA (J+3, K) are each connected to the bit line pairs arranged between a sense amplifier SA (J+2, K+1) in another ~~one~~ next line and a sense amplifier SA (J+3, K+1) ~~or between a sense amplifier SA (J+2, K-1) in the other next line and a sense amplifier SA (J+3, K-1)~~;

a sense amplifier SA (J+4, K) and a sense amplifier SA (J+5, K) are each connected to each of the bit line pairs arranged between a sense amplifier SA (J+4, K-1) in one next line and a sense amplifier SA (J+5, K-1) ~~or between a sense amplifier SA (J+4, K+1) in the other next line and a sense amplifier SA (J+4, K+1)~~; and

P and Q are both integers of more than 6, J is an arbitrary integer of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q.

PAGE 8/18 * RCVD AT 2/1/2005 2:47:45 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/6 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):04-48

15. (Original) An operation method of a DRAM circuit comprising a plurality of aligned sense amplifiers,

bit line pairs connected to the plurality of sense amplifiers, respectively, and

memory cells connected respectively to the bit lines constituting the bit line pairs, wherein

the bit line pairs and memory cells are alternately arranged on a right side (upper side) and a left side (lower side) of the sense amplifiers per N (N: natural number) aligned sense amplifiers,

the method comprising a step of activating the plurality of sense amplifiers connected to the bit line pairs and memory cells arranged on the right side (upper side) of the sense amplifiers, and the plurality of sense amplifiers connected to the bit line pairs and memory cells arranged on the left side (lower side) of the sense amplifiers at different timing, when data is read.

16. (Original) An operation method of a DRAM circuit comprising:

a plurality of sense amplifiers arranged in Q lines each containing the P sense amplifiers;

bit line pairs connected to the plurality of sense amplifiers, respectively; and

memory cells connected respectively to the bit lines constituting the bit line pairs,

wherein the bit line pairs and the memory cells are arranged every N (N: natural number) aligned sense amplifiers in the Q lines, alternately on a right side (upper side) and a left

PAGE 9/18 * RCVD AT 2/1/2005 2:47:45 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/6 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):04-48

side (lower side) of the sense amplifiers, and P and Q are both integers of more than 3, and N is an arbitrary integer of more than 1 and less than (P/3);

the method comprising a step of activating the plurality of sense amplifiers connected to the bit line pairs and memory cells arranged on the right side (upper side) of the sense amplifiers, and the plurality of sense amplifiers connected to the bit line pairs and memory cells arranged on the left side (lower side) of the sense amplifiers at different timing, when data is read.

17. (Original) An operation method of a DRAM circuit comprising:

a plurality of sense amplifiers SA (J, K) arranged in Q lines each containing the P sense amplifiers;

bit line pairs connected to the plurality of sense amplifiers SA (J, K), respectively; and

memory cells connected respectively to the bit lines constituting the bit line pairs,

wherein the sense amplifier SA (J, K) is connected to each of the bit line pairs arranged between the sense amplifier SA (J, K) and a sense amplifier SA (J, K-1) in one next line or a sense amplifier SA (J, K+1) in the other next line;

a sense amplifier SA (J+1, K) is connected to the bit line pair arranged between the sense amplifier SA (J+1, K) and a sense amplifier SA (J+1, K+1) in one next line or a sense amplifier SA (J+1, K-1) in the other next line;

a sense amplifier SA (J+3, K) is connected to the bit line pair arranged between the sense amplifier SA (J+3, K) and a sense amplifier SA (J+2, K-1) in one next line or a sense amplifier SA (J+2, K+1) in the other next line; and

PAGE 10/18 * RCVD AT 2/1/2005 2:47:45 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/6 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):04-48

P and Q are both integers of more than 3, J is an arbitrary integer of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q;

the method comprising a step of activating the sense amplifier SA (J+1, K) at timing different from the sense amplifier SA (J, K) and the sense amplifier SA (J+3, K), when data is read.

18. (Original) An operation method of a DRAM circuit comprising:

a plurality of sense amplifiers SA (J, K) arranged in Q lines each containing the P sense amplifiers;

bit line pairs connected to the plurality of sense amplifiers SA (J, K), respectively; and

memory cells connected respectively to the bit lines constituting the bit line pairs,

wherein sense amplifier SA (J, K) and a sense amplifier SA (J+1, K) are each connected to each of the bit line pairs arranged between a sense amplifier SA (J, K-1) in one next line and a sense amplifier SA (J+1, K-1) or between a sense amplifier SA (J, K+1) in the other next line and a sense amplifier SA (J+1, K+1);

a sense amplifier SA (J+2, K) and a sense amplifier SA (J+3, K) are each connected to the bit line pairs arranged between a sense amplifier SA (J+2, K+1) in one next line and a sense amplifier SA (J+3, K+1) or between a sense amplifier SA (J+2, K-1) in the other next line and a sense amplifier SA (J+3, K-1);

a sense amplifier SA (J+4, K) and a sense amplifier SA (J+5, K) are each connected to each of the bit line pairs arranged between a sense amplifier SA (J+4, K-1) in one next line and a sense amplifier SA (J+5, K-1) or between a sense amplifier SA (J+4, K+1) in the other next line and a sense amplifier SA (J+4, K+1); and

PAGE 11/18 * RCVD AT 2/1/2005 2:47:45 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/6 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):04-48

P and Q are both integers of more than 6, J is an arbitrary integer of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q;

the method comprising a step of activating the sense amplifier SA (J, K), the sense amplifier SA (J+1, K), the sense amplifier SA (J+4, K) and the sense amplifier SA (J+5, K) at timing different from the sense amplifier SA (J+2, K) and the sense amplifier SA (J+3, K), when data is read.

19. (New) A DRAM circuit comprising a plurality of aligned sense amplifiers,

bit line pairs connected to the plurality of sense amplifiers, respectively, and

memory cells connected respectively to the bit lines constituting the bit line pairs, wherein

the bit line pairs and the memory cells are alternately arranged on a right side (upper side) and a left side (lower side) of the sense amplifiers per N (N: natural number) aligned sense amplifiers so that first bit line pairs and memory cells are arranged on a right side (upper side) of a first sense amplifier, second bit line pairs and memory cells are arranged on a left side (lower side) of a second sense amplifier, third bit line pairs and memory cells are arranged on a right side (upper side) of a third sense amplifier, and so on until all bit line pairs and memory cells have been alternately arranged per the N aligned sense amplifiers.

20. (New) A DRAM circuit comprising:

a plurality of sense amplifiers arranged in Q lines each containing the P sense amplifiers;
bit line pairs connected to the plurality of sense amplifiers, respectively; and

memory cells connected respectively to the bit lines constituting the bit line pairs,

PAGE 12/18 * RCVD AT 2/1/2005 2:47:45 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/6 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):04-48

wherein the bit line pairs and the memory cells are arranged every N (N: natural number) aligned sense amplifiers in the Q lines, alternately on a right side (upper side) and a left side (lower side) of the sense amplifiers, and P and Q are both integers of more than 3, and N is an arbitrary integer of more than 1 and less than (P/3) so that first bit line pairs and memory cells are arranged on a right side (upper side) of a first sense amplifier in a first line, second bit line pairs and memory cells are arranged on a left side (lower side) of a second sense amplifier in a first line, third bit line pairs and memory cells are arranged on a right side (upper side) of a third sense amplifier in a first line, and so on until all bit line pairs and memory cells have been alternately arranged per the N aligned sense amplifiers in the Q lines.

PAGE 13/18 * RCVD AT 2/1/2005 2:47:45 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/6 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):04-48